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Compact Models and the Physics of Nanoscale FETs: Survey Paper

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ABSTRACT

This work discusses the compact model and the physics of nanoscale field-effect transistors (FETs), specifically the Virtual Source (VS) model. It points out how conventional compact models, originally formulated for microscale devices, can be extended to characterize nanoscale FETs by redefining fundamental parameters such as mobility and saturation velocity. The authors employ the Landauer method to give physical meaning to these parameters and demonstrate that transport in nanoscale FETs is diffusion-limited close to the virtual source, both below and above threshold. The work also addresses how current saturation is controlled by velocity saturation near the source instead of the maximum channel velocity and why conventional models are still valid even though the nanoscale has different transport mechanisms. The findings seek to close the gap between compact modeling and device physics, providing a better understanding of nanoscale FET behavior for both circuit design and research purposes.

KEYWORDS: *Virtual Source (VS) model, Landauer method, diffusion-limited transport, current saturation, velocity saturation*

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INTRODUCTION

The success of circuit simulation relies on the creation of compact models that reconcile theoretical correctness with CAD implementation. The article focuses on asymptotically correct models that are physically valid even at extreme operating conditions such as high bias or temperature. Smooth, continuous formulations are essential for numerical stability to prevent convergence problems in transient and distortion analyses that afflict discontinuous models. Layout dependent effects need to be included in order to account for parasitic resistances and capacitances that have a significant impact on simulation accuracy. Physically-based models that are linked to process parameters allow for more effective statistical modeling than empirical methods, specifically for mismatch analysis. The work violates usual characterization practice by demonstrating how assuming the measured and model parameters are equal causes measurement approximation errors. Practical Use demands models to operate without issues throughout the entire design flow from schematic to layout verification. Finally, the paper presents a broad framework for building strong models that span theoretical physics to practical design needs.[1]

This paper introduces a high-performance non-quasi-static(NQS) MOSFET model for simulation of circuits that corrects shortcomings of conventional quasi-static (QS) models unable to correctly forecast high-frequency and fast transient characteristics. By the introduction of channel charge relaxation mechanisms in the form of an Elmore RC approximation, the model correctly accounts for finite carrier charging times, eradicating physical spikes in current and convergence problems during simulations. The model retains computational performance with under 30% runtime overhead while ensuring compatibility with current BSIM3 platforms. Verification against PISCES simulations exhibits excellent consistency in transient and AC small-signal analysis, eliminating differences observed in Q models, e.g., erroneous trans admittance predictions. Realistic implementations, such as a high- speed DAC cell, reflect the model's capability to unmask intrinsic speed limits obscured by approximations. The design strikes a balance between precision and

usability, providing a scalable solution for contemporary IC design without the need for intricate parameter extraction or topology modification. This innovation fills an essential gap in MOSFET modeling for high-speed circuits near device cut-off frequencies.[2]

This paper explores the fundamental importance of diffusion current in the operation of MOS transistors, showing that it is a determining factor in the accurate modeling of current saturation. The authors present a full theory integrating drift and diffusion currents within a one-dimensional gradual channel approach, and it is in strong agreement with experiment over all regions of operation. Their work demonstrates how diffusion current prevails in proximity to pinch-off regions, allowing for accurate current continuity and saturation behavior not predicted by drift-only models. The research gives comprehensive explanations of surface potential distribution, quasi-Fermi levels, and electric field variations along the channel for various bias conditions. It also studies major dynamic characteristics such as gate capacitance, transconductance, and drain conductance and provides better understanding of device operation. These results set the cornerstone principles that have guided current MOSFET modeling techniques.[3]

The present research investigates the ultimate scaling frontiers of silicon MOSFET technology using Monte Carlo simulations of a 30 nm dual-gate transistor. The work shows that dual-gate structures can deliver outstanding performance figures, such as a transconductance of 2300 mS/mm and sub-picosecond switching time, while suppressing short-channel effects. Major findings indicate near-ballistic electron transport with peak velocities of 2.7×10^7 cm/s supported by the ultrathin 5 nm channel structure. The paper emphasizes key technological challenges to achieving such scaled devices, such as thickness control, dual-gate alignment, and thermal management solutions. Resistively-loaded inverter simulations project ring oscillator delays as low as 1.1ps, demonstrating the promise of future high-speed digital applications. These findings set basic performance benchmarks for nanoscale MOSFETs at the physical limits of silicon technology.[4]

Li-passivation in zigzag GaN nanoribbons significantly modifies their electronic properties, enhancing Fermi velocity and reducing effective mass to improve carrier mobility. DFT investigations further show strong gas adsorption and charge transfer, highlighting their potential as high-performance nanosensors[5-6].

This work explores the underlying physics of carrier transport in nanoscale MOSFETs with extensive numerical simulations of a 10 nm double-gate transistor. The work proves that current conduction is controlled by thermal injection velocity at the source and backscattering in a critical "kT-layer" close to the channel entrance, instead of standard drift-diffusion processes. Key results indicate carrier degeneracy raises injection speeds above classical thresholds, whereas MOS electrostatics preserves near-equilibrium charge densities at the source barrier even in strongly non-equilibrium transport conditions. The study formulates a quasi-ballistic transport paradigm in which scattering within only the first 1-2 nm of the channel dictates total device performance. These findings offer a simplified but correct physical description of nanoscale MOSFET operation, filling the gap between sophisticated quantum simulations and realistic compact modeling requirements for future devices.[7]

MOSFET compact modeling is a field of wide-ranging study with widely differing models existing in both terms of complexity and accuracy; most models tend to be hierarchically organized starting from basic carrier charge and transport models which them selves may incorporate many levels of description. Although most of these models are used for the purpose of computer-aided design, with an emphasis on accurate and detailed fittings to device characteristics in various geometries and layouts, this paper presents a model aimed at providing a simple and straightforward understanding of carrier transport in modern short-channel planar MOSFETs. This main objective encompasses facilitating the extraction of important parameters like the virtual source carrier velocity. The hereinafter presented semiempirical model successfully captures the current-to-voltage behavior in short-channel MOSFETs across all operating regimes such that there exists a continuous description of both current and its derivatives. Simplicity and sufficient accuracy are ensured by modeling from the fundamental physics of short-channel device transport using a minimal number of physical parameters that are easily accessible or even known inherently. A fundamental contribution of this work is the model's ability to retrieve the virtual-source carrier velocity, a variable of high technological relevance.[8]

This work presents a backscattering model that is suitable for nanoscale MOSFETs' compact modeling using the Landauer flux-scattering theory. The model is to explain quasi-ballistic transport by precisely calculating ballistic and backscattering probabilities within the channel. The model is to overcome the

shortcomings of conventional compact models are no longer valid when silicon MOSFET channel lengths drop below 50 nm. Traditional models, using drift-diffusion theory and statistical mobility, are unable to model transistor operation near the ballistic limit in state-of-the-art MOSFETs. Traditional models rely on a shifted Maxwellian distribution function, which is in appropriate when channel length and mean-free path are on the same order. The new model overcomes the limitations of the compact modeling method by employing the Landauer theory, under which continuity can be achieved between drift-diffusion and ballistic transport regimes. One of the central factors in this theory is the backscattering coefficient, which is associated with the extent of transport ballisticity.[9]

DFT-based studies demonstrate that Indium Nitride nanoribbons can effectively detect gases like CO, CO_2, NO, and NO_2 due to notable charge transfer and band structure modulation. Similarly, Scandium Nitride monolayers show strong adsorption sensitivity toward toxic gases such as NH_3, AsH_3, BF_3, and BCl_3. Zigzag silicon carbide nanoribbons exhibit enhanced gas sensing performance through improved electronic response to hazardous gas molecules, making them promising for advanced sensor applications[10-12].

This work examines the theoretical underpinnings of the kT-layer theory applied to carrier transport in quasi-ballistic nanoscale devices. The authors establish analytical solutions to the backscattering coefficient based on a one-dimensional Boltzmann transport equation under a "relaxation length" assumption. The outcomes are consistent with empirical equations from Lundstrom Tal., bridging the gap between low- and high-field conditions. The research emphasizes the hypotheses underlying these equations, including non degenerate statistics and reduced- scattering models, and their limitations. The results shed light on the contribution of scattering close to the source in nanoscale MOSFETs and present a framework for compact model extension to quasi-ballistic transport. The research highlights the significance of the kT-layer concept to comprehend and optimize device performance.[13]

Density Functional Theory (DFT) investigations reveal that Cu and Fe doping in boron nitride nanoribbons (BNNRs) significantly enhances their electrical conductivity, making them suitable candidates for nanoscale interconnects in advanced integrated circuits. Ab-initio studies on aluminum nitride nanoribbons (AlNNRs) demonstrate their potential in implementing reconfigurable logic gates due to tunable electronic properties under external stimuli. Additionally, the design of a FinFET-based operational amplifier (Op-Amp) using 22 nm high-k dielectric technology shows promising results in reducing leakage currents and enhancing performance, offering a robust solution for low-power, high-efficiency analog circuit applications[14-16].

This paper provides an overview of the principles that guide phonon transport, a key phenomenon in heat flow in solid-state materials. The main emphasis is on how lattice vibrations, or phonons, are responsible for thermal conduction, particularly in semiconductors and insulators. The paper makes Comparisons With Electron transport while also highlighting important differences in their behavior. Concepts such as dispersion relations and group velocity are introduced to lay the groundwork for the analysis of electron and phonon transport. In Addition, the lecture formulates a general theory of heat conduction, introducing key quantities such as heat flux and thermal conductivity. Lastly, itdiscusses simplified models such as the Debye model and the impact of scattering mechanisms on phonon transport.[17]

This work examines electron transport in nanometer Si MOSFETs by employing the magnetoresistance technique. Monte Carlo simulation is used to explore electron transport within these nanometer MOSFETs using real device parameters. The calculated values of mobility and transmission coefficient match experimental findings and are proved to be functions of electron concentration. Scattering event analysis and time of flight both show indications of ballistic motion in these structures, which affect mobility deterioration short transistors. The Results validate the applicability of the interpretation of the magnetoresistance coefficient as mobility squared, even in situations involving quasi ballistic electron transport.[18]

This paper presents the physics of electronic transport in nMOSFETs at the 10-nm node. It deals with long-range Coulomb interactions that ca impair performance and limit ballistic transport. The research also investigates scattering with high-k insulator interfacial modes, which diminishes electron mobility. It also discusses the applicationofhigh-mobilitysmalleffective-masssubstrates,highlighting concerns regarding limitations to performance based on the density-of-states(DOS) bottleneck and band-to-band (Zener) leakage current. The paper concludes that ballistic transport can be unrealizable and impractical owing to electron-electron collisions. It also claims that low-field mobility is possibly not beneficial to the prediction of device performance at the saturated regime.[19]

This work covers the physics of electronic transport in 10-nm scale nMOSFETs, overcoming challenges that occur at such dimensions. It discusses long-range Coulomb interactions, which can reduce performance and limit ballistic transport, and scattering with high-k insulator interfacial modes, which lowers electron mobility. The work also discusses the application of high-mobility substrates, taking into account limitations because of the density-of-states bottleneck and band-to- band leakage current. The authors present the argument that ballistic transport might be impossible and even undesirable with electron-electron collisions and point out that low-field mobility would not be the best indicator of device performance in the saturated region.[20]

With silicon MOSFETs decreasing further into the nanometer range, electron transport behavior becomes ever more critical for device optimization. This article explores electron mobility in such extremely small devices, down to gate lengths of30 nm, through the highly sensitive magnetoresistance method. The experimental results are then compared with detailed Monte Carlo simulations that account for the complexity of nanoscale device physics. Based on the analysis of experimental measurements and simulation outcomes, this research yields insights into the effect of lowered dimensions on electron mobility as well as the occurrence of Quasi ballistic transport phenomena in high-performance MOSFETs.[21]

This work enters the domain of MOSFET physics to examine the influence of carrier scattering on MOSFET behavior, as practical MOSFETs operate below the theoretical ballistic limit because of these interactions. The main goal of this text is to promote a deep comprehension of how different scattering processes impact transistor properties and eventually build an advanced model that goes beyond the reduced context represented in equation. Through the investigation of the departures from ballistic transport due to scattering, the chapterhopest give more realistic and useful approach to analyzing and predicting the behavior of nanoscale MOSFETs under actual operating situations.[22]

The analysis utilizes a quantum mechanical, ballistic transport model together with a 2D Poisson solver to calculate device performance characteristics including drain- induced barrier lowering (DIBL), subthreshold swing (SS), and on-current. Simulations identify that the 60nm devices approach the ballistic limit when parasitic series resistance is included, although on-currents are overestimated by the ballistic model, especially at high gate voltages. Among key findings are the identification of source design constraints and conduction band nonparabolicity as sources of performance limitations, and the influence of semiconductor capacitance of gate control. The paper indicates the problems involved in III-V HEMT scaling and underscores the impact of series resistance, source optimization, and insulator thickness to produce better device performance. In general, the work sheds light on the near-ballistic operation of III-V HEMTs and points to important areas of further investigation.[23]

This work presents a reduced analytical theory for ballistic transistors based on insights from numerical simulations. The theory can be applied to both traditional MOSFETs and new unconventional field-effect transistors. It includes 2-D electrostatics and the quantum capacitance limit, and it gives a framework for explaining MOSFET performance as scaling approaches its limits. The research highlights the increasing significance of ballistic transport in transistors with sub-10 nm channel lengths.[24].

Conclusion

This work examines the physics of nanoscale field-effect transistors (FETs) and its connection with conventional compact models. It emphasizes the strength of the Virtual Source (VS) model in modeling nanoscale FETs through the reinterpretation of important parameters such as mobility and saturation velocity. The research stresses that transport in nanoscale FETs is intrinsically different from microscale devices, with diffusion at the vicinity of the virtual source being pivotal to current saturation. The Landauer methodology offers a direct physical interpretation for the parameters in terms of ballistic and quasi-ballistic transport mechanisms. The conclusion of the paper is that although existing models can be made to fit experimental data, interpreting the physics behind is vital for correct device interpretation and model development in the future. It also points to the difficulty in developing fully predictive models bridging long-channel and nanoscale FET behavior. The information provided is intended to inform device research and compact modeling for next-generation semiconductor technologies.

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